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1. Multiple-banked register file architectures

Cruz, J.-L.; Gonzalez, A.; Valero, M.; Topham, N.P.;
 Computer Architecture, 2000. Proceedings of the 27th International Symposium on
 2000 Page(s):316 - 325

AbstractPlus | Full Text: PDF(800 KB) IEEE CNF
[Rights and Permissions](#)

2. MARS-a RISC-based architecture for LISP

Hung-Chang Lee; Felipe Lai; Jenn-Yuan Tsai; Tai-Ming Pang; Yu-Gang Li;
 Tools for Artificial Intelligence, 1989. Architectures, Languages and Algorithms. IEEE International
 23-25 Oct. 1989 Page(s):198 - 206
 Digital Object Identifier 10.1109/TAI.1989.65321

AbstractPlus | Full Text: PDF(788 KB) IEEE CNF
[Rights and Permissions](#)

3. Early Register Deallocation Mechanisms Using Checkpointed Register Files

Ergin, O.; Balkan, D.; Ponomarev, D.; Ghose, K.;
 Computers, IEEE Transactions on
 Volume 55, Issue 3, Sept. 2006 Page(s):1153 - 1166
 Digital Object Identifier 10.1109/TC.2006.145

AbstractPlus | Full Text: PDF(6408 KB) IEEE JNL
[Rights and Permissions](#)

4. MARS: a RISC based multiple function units LISP machine

Lee, H.-C.; Lai, F.; Pang, T.-M.;
 Computers and Digital Techniques, IEE Proceedings-
 Volume 139, Issue 5, Sep 1992 Page(s):410 - 420

AbstractPlus | Full Text: PDF(784 KB) IET JNL

5. Increasing processor performance through early register release

Ergin, O.; Balkan, D.; Ponomarev, D.; Ghose, K.;
 Computer Design: VLSI in Computers and Processors, 2004. ICCD 2004. Proceedings. IEEE Int'l
 11-13 Oct. 2004 Page(s):480 - 487
 Digital Object Identifier 10.1109/ICCD.2004.1347965

[AbstractPlus](#) | [Full Text: PDF\(327 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

6. Design considerations and implementations of a high performance dynamic register file

Joshi, R.V.; Hwang, W.;
VLSI Design, 1999. Proceedings, Twelfth International Conference On
 7-10 Jan. 1999 Page(s):526 - 531
 Digital Object Identifier 10.1109/ICVD.1999.745208

[AbstractPlus](#) | [Full Text: PDF\(984 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

7. Teaching computer architecture/organisation using simulators

Grunbacher, H.;
Frontiers in Education Conference, 1998. FIE '98, 28th Annual
 Volume 3, 4-7 Nov. 1998 Page(s):1107 - 1112 vol.3
 Digital Object Identifier 10.1109/FIE.1998.738576

[AbstractPlus](#) | [Full Text: PDF\(1664 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

8. A scalable register file architecture for dynamically scheduled processors

Wallace, S.; Bagherzadeh, N.;
Parallel Architecture and Compilation Techniques, 1998., Proceedings of the 1998 Conference on
 20-23 Oct. 1998 Page(s):179 - 184
 Digital Object Identifier 10.1109/PACT.1998.552666

[AbstractPlus](#) | [Full Text: PDF\(604 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

9. Overview of the PIPE processor implementation

Farens, M.K.; Pleszkun, A.R.;
System Sciences, 1991. Proceedings of the Twenty-Fourth Annual Hawaii International Conference on
 Volume 1, 8-11 Jan. 1991 Page(s):433 - 443 vol.1
 Digital Object Identifier 10.1109/HICSS.1991.183913

[AbstractPlus](#) | [Full Text: PDF\(860 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

10. An eight-issue tree-VLIW processor for dynamic binary translation

Ebcioğlu, K.; Fritts, J.; Kosonocky, S.; Geschwind, M.; Altman, E.; Kallias, K.; Bright, T.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings, International
 5-7 Oct. 1998 Page(s):486 - 495
 Digital Object Identifier 10.1109/ICCD.1998.727094

[AbstractPlus](#) | [Full Text: PDF\(108 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

11. High-performance and low-cost dual-thread VLIW processor using Weld architecture paradigm

Ozer, E.; Conte, T.M.;
Parallel and Distributed Systems, IEEE Transactions on
 Volume 16, Issue 12, Dec. 2005 Page(s):1132 - 1142
 Digital Object Identifier 10.1109/TPDS.2005.150










[AbstractPlus](#) | [Full Text: PDF\(1440 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)

12. Dynamically allocating processor resources between nearby and distant ILP

Balasubramanian, R.; Dwarkadas, S.; Albonesi, D.H.;
Computer Architecture, 2001. Proceedings, 28th Annual International Symposium on
 30 June-4 July 2001 Page(s):26 - 37
 Digital Object Identifier 10.1109/ISCA.2001.937428

[AbstractPlus](#) | [Full Text: PDF\(200 KB\)](#) | [IEEE C&NF](#)
[Rights and Permissions](#)

13. Predicting and Exploiting Transient Values for Reducing Register File Pressure and Energy

-  **Balkan, Deniz; Sharkey, Joseph; Ponomarev, Dmitry V.; Ghose, Kanad.**
Transactions on Computers
 Volume 57, Issue 1, Jan. 2008 Page(s):82 - 95
 Digital Object Identifier 10.1109/TC.2007.70785
[AbstractPlus](#) | [Full Text: PDF\(795 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  **14. A 0.18 μ m CMOS IA32 microprocessor with a 4 GHz integer execution unit**
 Sager, D.; Hinton, G.; Upton, M.; Chappell, T.; Fletcher, T.D.; Samaan, S.; Murray, R.;
Solid-State Circuits Conference, 2001. Digest of Technical Papers, ISSCC, 2001 IEEE International
 5-7 Feb. 2001 Page(s):324 - 325, 461
 Digital Object Identifier 10.1109/ISSCC.2001.912656
[AbstractPlus](#) | [Full Text: PDF\(188 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  **15. Delaying physical register allocation through virtual-physical registers**
 Monreal, T.; Gonzalez, A.; Valero, M.; Gonzalez, J.; Vinals, V.;
Microarchitecture, 1999. MICRO-32. Proceedings, 32nd Annual International Symposium on
 16-18 Nov. 1999 Page(s):186 - 192
 Digital Object Identifier 10.1109/MICRO.1999.809456
[AbstractPlus](#) | [Full Text: PDF\(48 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  **16. The Intel IA-64 compiler code generator**
 Bharadwaj, J.; Chen, W.Y.; Chuang, W.; Hollehnner, G.; Menezes, K.; Muthukumar, K.; Pierce, J.;
Micro, IEEE
 Volume 20, Issue 5, Sept.-Oct. 2000 Page(s):44 - 53
 Digital Object Identifier 10.1109/40.877949
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(164 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  **17. VIPER: a VLIW integer microprocessor**
 Gray, J.; Naylor, A.; Abnous, A.; Bagherzadeh, N.;
Solid-State Circuits, IEEE Journal of
 Volume 28, Issue 12, Dec. 1993 Page(s):1377 - 1382
 Digital Object Identifier 10.1109/4.262015
[AbstractPlus](#) | [Full Text: PDF\(564 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  **18. New hardware scheme supporting precise exception handling for out-of-order execution**
 Hwang, G.C.; Kyung, C.M.;
Electronics Letters
 Volume 30, Issue 1, 6 Jan. 1994 Page(s):16 - 17
[AbstractPlus](#) | [Full Text: PDF\(192 KB\)](#) | [IEE JNL](#)
-  **19. Using a resource-limited instruction scheduler to evaluate the iHARP processor**
 Steven, F.L.; Steven, G.B.; Wang, L.;
Computers and Digital Techniques, IEEE Proceedings,
 Volume 142, Issue 1, Jan. 1995 Page(s):23 - 31
[AbstractPlus](#) | [Full Text: PDF\(656 KB\)](#) | [IEE JNL](#)
-  **20. Analytical models for leakage power estimation of memory array structures**
 Mamidipaka, M.; Khouri, K.; Dutt, N.; Abadir, M.;
Hardware/Software Codesign and System Synthesis, 2004. CODES + ISSS 2004. International C
 2004 Page(s):146 - 151
[AbstractPlus](#) | [Full Text: PDF\(560 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  **21. Revolver: a high-performance MIMD architecture for collision free computing**
 Oberg, J.; Elvelev, P.;

[Eurosimo Conference, 1996, Proceedings, 24th](#)
Volume 1, 25-27 Aug. 1996 Page(s) 301 - 308 vol.1
Digital Object Identifier 10.1109/EURMIC.1996.711814
[AbstractPlus](#) | [Full Text: PDF](#) (596 KB) | [IEEE CNF](#)
[Rights and Permissions](#)

22. Formal verification of memory arrays using symbolic trajectory evaluation

Pandey, M.; Bryant, R.E.;
[Memory Technology, Design and Testing, 1997. Proceedings., International Workshop on](#)
11-12 Aug. 1997 Page(s) 42 - 49
Digital Object Identifier 10.1109/MTDT.1997.619393
[AbstractPlus](#) | [Full Text: PDF](#) (708 KB) | [IEEE CNF](#)
[Rights and Permissions](#)

23. Performance evaluation of the PowerPC 620 microarchitecture

Diep, T.A.; Nelson, C.; Shen, J.P.;
[Computer Architecture, 1995. Proceedings. 22nd Annual International Symposium on](#)
22-24 Jun 1995 Page(s) 163 - 174
[AbstractPlus](#) | [Full Text: PDF](#) (1120 KB) | [IEEE CNF](#)
[Rights and Permissions](#)

24. Illustration of the SFG-tracing multi-level behavioral verification methodology, by the core level synthesis application in Cathedral-II

Genoe, M.; Claesen, L.; Verind, E.; Proesmans, F.; De Man, H.;
[Computer Design: VLSI in Computers and Processors, 1991. ICCD '91. Proceedings., 1991 IEEE](#)
14-16 Oct. 1991 Page(s) 338 - 341
Digital Object Identifier 10.1109/ICCD.1991.139913
[AbstractPlus](#) | [Full Text: PDF](#) (412 KB) | [IEEE CNF](#)
[Rights and Permissions](#)

25. VIPER: A 25-MHz, 100-MIPS peak VLIW microprocessor

Gray, J.; Naylor, A.; Abnous, A.; Bagherzadeh, N.;
[Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE, 1993](#)
9-12 May 1993 Page(s) 4.1.1 - 4.1.5
Digital Object Identifier 10.1109/CICC.1993.590396
[AbstractPlus](#) | [Full Text: PDF](#) (536 KB) | [IEEE CNF](#)
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